TED (15) – 3042 Reg. No. .....

(REVISION — 2015) Signature .....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — APRIL, 2018

DIGITAL ELECTRONICS

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. Give any two alphanumeric codes.
2. What is a combinational logic circuit ? Give an example.
3. What is the basic difference between a latch and a flip-flop ?
4. Define resolution of a DAC.
5. Give the output expressions of a half adder circuit.

(5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Briefly explain excess-3 codes and gray coles.
2. Explain the operation of a 4 to 1 multiplexer.
3. Explain a parallel adder with diagram.
4. Distinguish between synchronous and asynchronous counters.
5. Implement AND, OR and XOR gates using NAND gate only.
6. Explain the working of a serial in serial out shift register with diagram.
7. Explain a counter type ADC.

(5×6 = 30)

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) Perform the following conversions.

(i) $(C5E2)_{16} = (\ldots\ldots)_2$ (ii) $(9AF)_{16} = (\ldots\ldots)_{10}$

(iii) $(110.001)_2 = (\ldots\ldots)_{10}$ (iv) $(11.75)_{10} = (\ldots\ldots)_2$ 8

(b) Perform : (i) – 43 + (–78) (ii) + 83 – (+16) using binary arithmetic. 7

OR

IV (a) Minimize the following function using K-map and realize using logic gates.

$F = \Sigma m (0, 1, 2, 5, 8, 10, 11, 14, 15)$ 10

(b) Write short note on BCD code. 5

UNIT — II

V (a) Design a 4 bit binary to gray code converter. 12

(b) Explain the levels of integration : SSI, MSI, VLSI. 3

OR

VI (a) Define the terms - V_{IL}, V_{OH}, V_{OL}, V_{OH}. 8

(b) Compare ECL and CMOS logic families. 7

UNIT — III

VII (a) Draw and explain SR flip flop using NAND gates. 8

(b) With necessary diagrams explain a 4 bit ring counter. 7

OR

VIII (a) Draw and explain JK flip flop with NAND gates. 8

(b) Explain the synchronous and asynchronous inputs of flip-flops. 7

UNIT — IV

IX (a) Draw and explain a mod-8 synchronous counter using JK flip-flops. 9

(b) Explain the working of a 4 bit weighted resistor type DAC. 6

OR

X (a) Explain a successive approximation ADC with diagram. 10

(b) Draw and explain the truth table of a mod-8 up/down counter. 5